

DATA SHEET

74F862, 74F863 **Bus transceivers (3-State)**

Product specification
Supersedes data of 1999 Jan 08
IC15 Data Handbook

2000 Mar 24

Bus transceivers (3-State)

74F862, 74F863

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- I_{IL} is 20µA vs. 1000µA for AM29861 series
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim dual In-line (DIP) 300mil package
- Broadside pinout compatible with AMD AM29862–29863
- Outputs sink 64mA

DESCRIPTION

The 74F862 and 74F863 bus transceivers provide high performance bus interface buffering for wide data/address paths of buses carrying parity. The 74F863 9-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F862	6.0ns	150mA
74F863	6.0ns	115mA

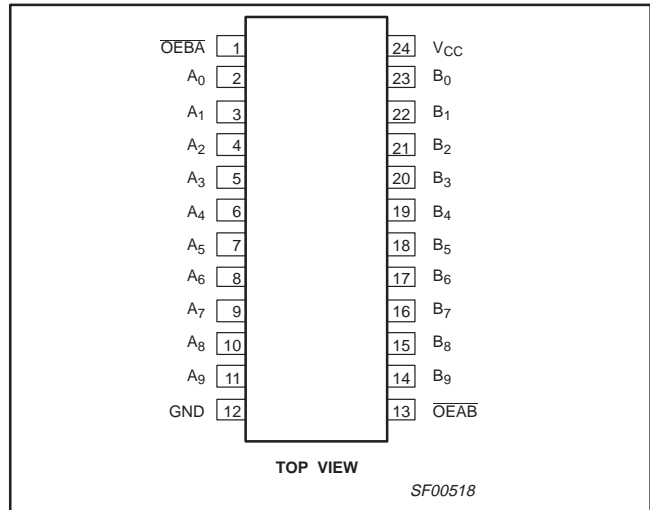
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_a = 0^\circ C$ to $+70^\circ C$	PKG DWG #
24-pin Plastic Slim Dual In-line (300mil) Package	N74F862N, N74F863N	SOT222-1
24-pin Plastic Small Outline Large ¹	N74F862D, N74F863D	SOT137-1

NOTE:

1. Thermal mounting techniques are recommended. See SMD Process Applications for a discussion of thermal considerations for surface mounted devices.

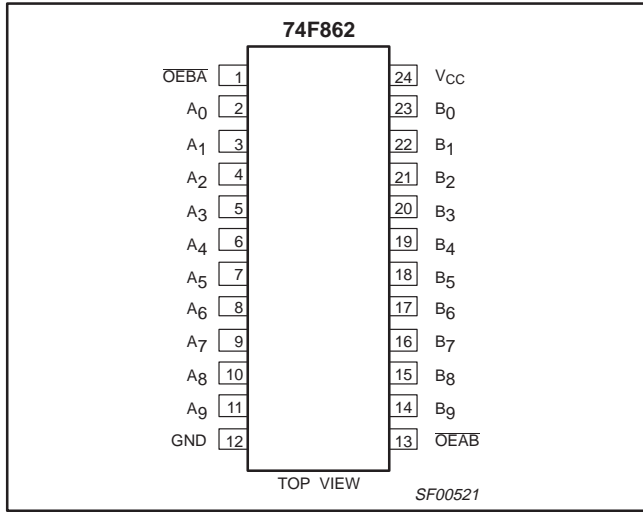
PIN CONFIGURATION



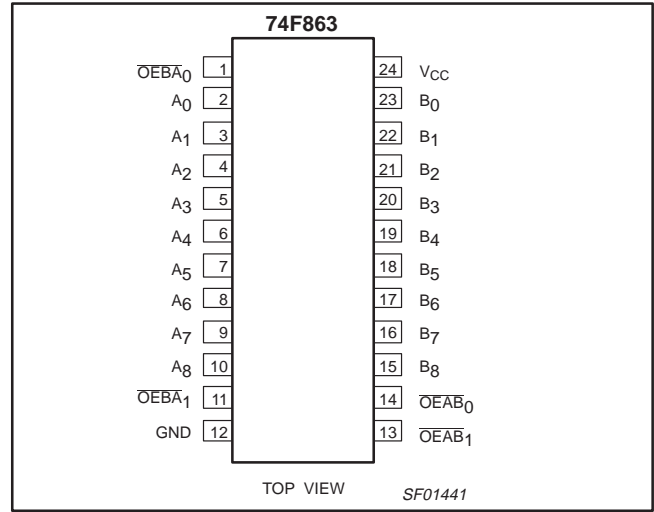
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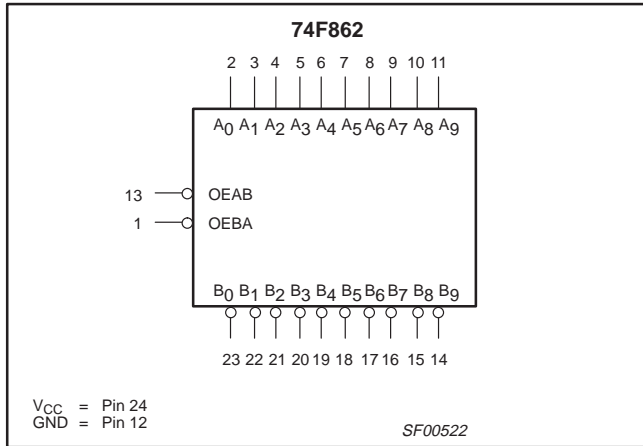
PIN CONFIGURATION



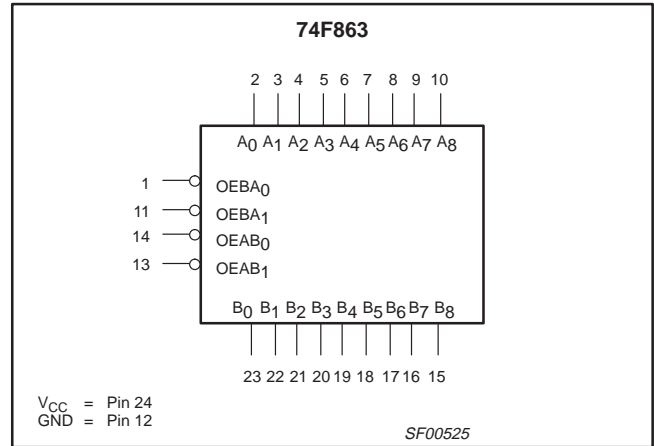
PIN CONFIGURATION



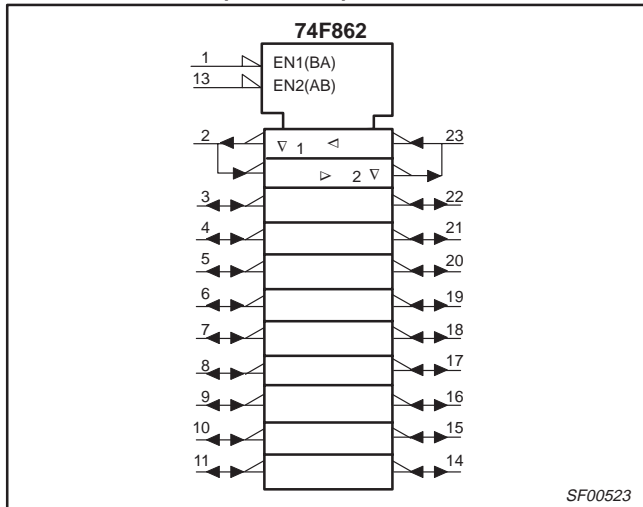
LOGIC SYMBOL



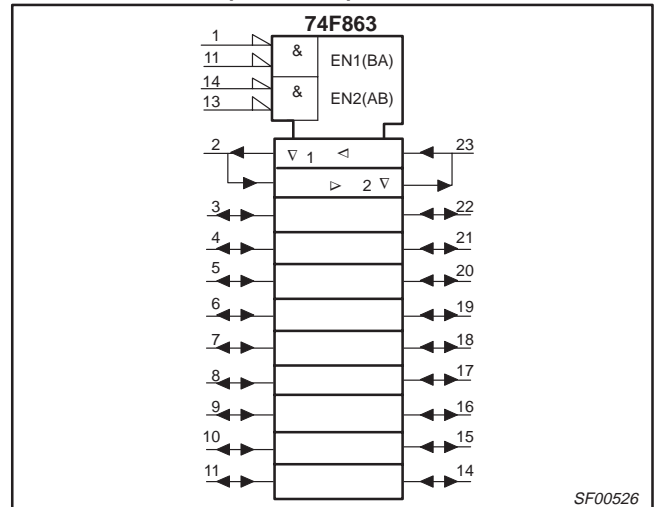
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



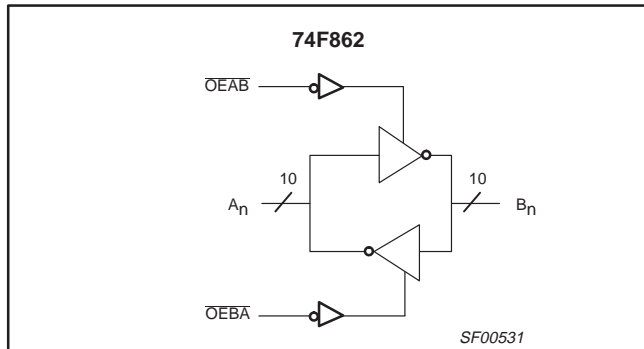
LOGIC SYMBOL (IEEE/IEC)



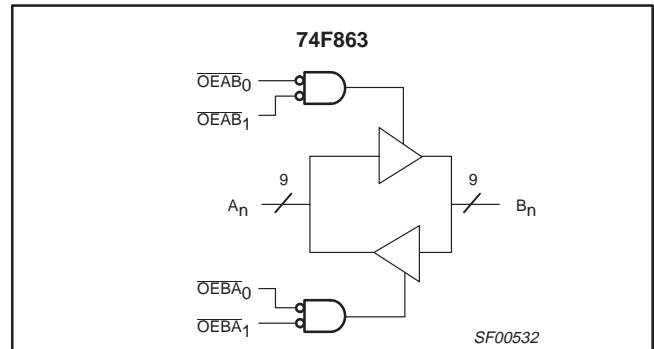
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LOGIC DIAGRAM



LOGIC DIAGRAM



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F862	A ₀ – A ₉	Data transmit inputs	3.5/0.117	70µA/70µA
	B ₀ – B ₉	Data receive inputs	3.5/0.117	70µA/70µA
	\overline{OEBA}	Transmit output enable input	1.0/0.033	20µA/20µA
	\overline{OEAB}	Receive output enable input	1.0/0.033	20µA/20µA
	A ₀ – A ₉	Data transmit outputs	1200/106.7	24mA/64mA
	B ₀ – B ₉	Data receive outputs	1200/106.7	24mA/64mA
74F863	A ₀ – A ₉	Data transmit inputs	3.5/0.117	70µA/70µA
	B ₀ – B ₉	Data receive inputs	3.5/0.117	70µA/70µA
	\overline{OEBA}_n	Transmit output enable input	1.0/0.033	20µA/20µA
	\overline{OEAB}_n	Receive output enable input	1.0/0.033	20µA/20µA
	A ₀ – A ₉	Data transmit outputs	1200/106.7	24mA/64mA
	B ₀ – B ₉	Data receive outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FUNCTION TABLE FOR 74F862

INPUTS		OPERATING MODES
\overline{OEAB}	\overline{OEBA}	74F862
L	H	A data to B bus
H	L	B bus to A data
H	H	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

FUNCTION TABLE FOR 74F863

INPUTS				OPERATING MODES
\overline{OEAB}_0	\overline{OEAB}_1	\overline{OEBA}_0	\overline{OEBA}_1	74F863
L	L	H	X	A data to B bus
L0	L	X	H	
H	X	L	L	B bus to A data
X	H	L	L	
H	H	H	H	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_a	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_a	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT	
						MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -1 mA	±10%V _{CC}	2.4			V	
					±5%V _{CC}	2.4	3.3		V	
			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -24 mA	±10%V _{CC}	2.0			V	
					±5%V _{CC}	2.0			V	
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = -48 mA	±10%V _{CC}		0.38	0.55	V	
				I _{OL} = 64 mA	±5%V _{CC}		0.42	0.55	V	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V	
I _I	Input current at maximum input voltage	$\overline{OEAB}, \overline{OEBA}$ $\overline{OEAB}_n, \overline{OEBA}_n$	V _{CC} = 0.0 V, V _I = 7.0 V					100	μA	
		A _n , B _n	V _{CC} = 5.5 V, V _I = 5.5 V					1	mA	
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V					20	μA	
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5 V					-20	μA	
I _{IH} + I _{OZH}	Off-state output current High-level voltage applied	A _n , B _n	V _{CC} = MAX, V _O = 2.7 V					70	μA	
			V _{CC} = MAX, V _O = 0.5 V					-70	μA	
I _{IL} + I _{OZL}	Off-state output current Low-level voltage applied	A _n , B _n	V _{CC} = MAX, V _O = 2.7 V					70	μA	
			V _{CC} = MAX, V _O = 0.5 V					-70	μA	
I _{OS}	Short-circuit output current ³		V _{CC} = MAX			-100		-225	mA	
I _{CC}	Supply current total	74F863	I _{CCH}	V _{CC} = MAX				145	195	mA
			I _{CCL}					140	195	mA
			I _{CCZ}					165	220	mA
		74F862	I _{CCH}					90	130	mA
			I _{CCL}					120	170	mA
			I _{CCZ}					130	160	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_a = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F863					UNIT
			T _a = +25°C V _{CC} = 5 V C _L = 50 pF, R _L = 500 Ω			T _a = 0°C to +70°C V _{CC} = 5 V ±10% C _L = 50 pF, R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A _n or B _n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t _{PLH} t _{PHL}	Propagation delay B _n or A _n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t _{PZH} t _{PZL}	Output Enable time High or Low level $\overline{OE}B_{A_n}$ to A _n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.5 10.0	5.0 4.0	13.0 11.0	ns
t _{PZH} t _{PZL}	Output Enable time High or Low level $\overline{OE}A_{B_n}$ to B _n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.0 10.0	5.0 4.0	13.0 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable time High or Low level $\overline{OE}B_{A_n}$ to A _n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t _{PHZ} t _{PLZ}	Output Disable time High or Low level $\overline{OE}A_{B_n}$ to B _n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

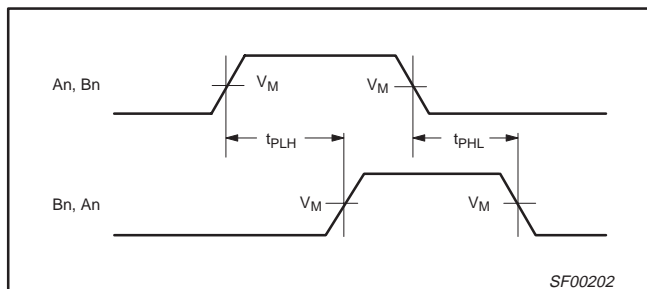
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F862					UNIT
			T _a = +25°C V _{CC} = 5 V C _L = 50 pF, R _L = 500 Ω			T _a = 0°C to +70°C V _{CC} = 5 V ±10% C _L = 50 pF, R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A _n or B _n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.0 7.0	ns
t _{PLH} t _{PHL}	Propagation delay B _n or A _n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.5 1.5	10.0 7.0	ns
t _{PZH} t _{PZL}	Output Enable time High or Low level $\overline{OE}B_{A_n}$ to A _n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t _{PZH} t _{PZL}	Output Enable time High or Low level $\overline{OE}A_{B_n}$ to B _n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t _{PHZ} t _{PLZ}	Output Disable time High or Low level $\overline{OE}B_{A_n}$ to A _n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time High or Low level $\overline{OE}A_{B_n}$ to B _n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

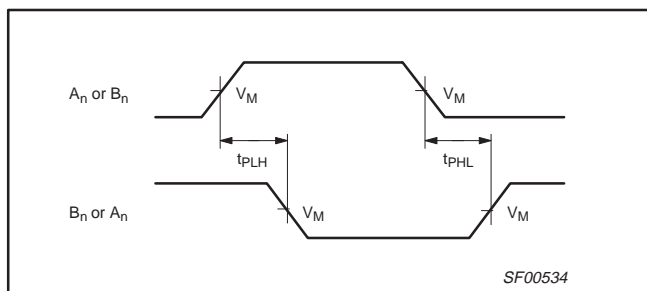
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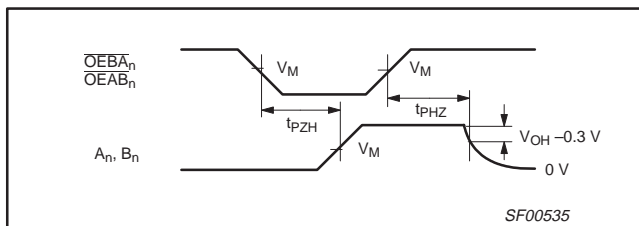
AC WAVEFORMS



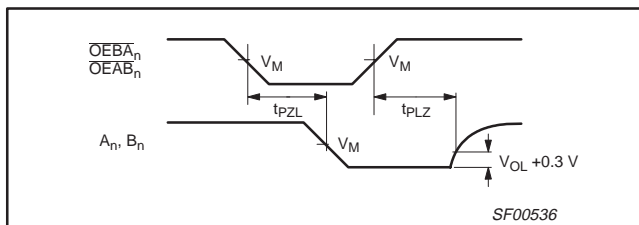
Waveform 1. Propagation Delay for Non-inverting Output



Waveform 2. Propagation Delay for Inverting Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUITS AND WAVEFORMS

Test Circuit for Open Collector Outputs

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

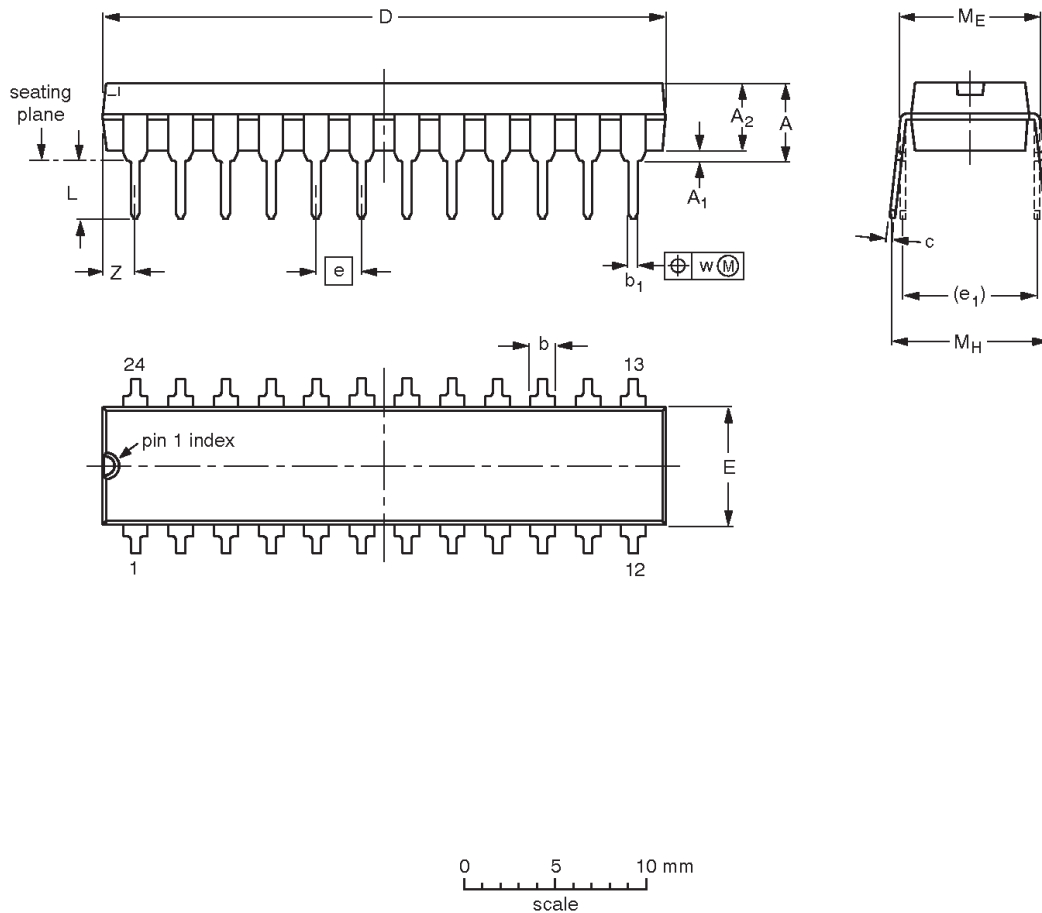
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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

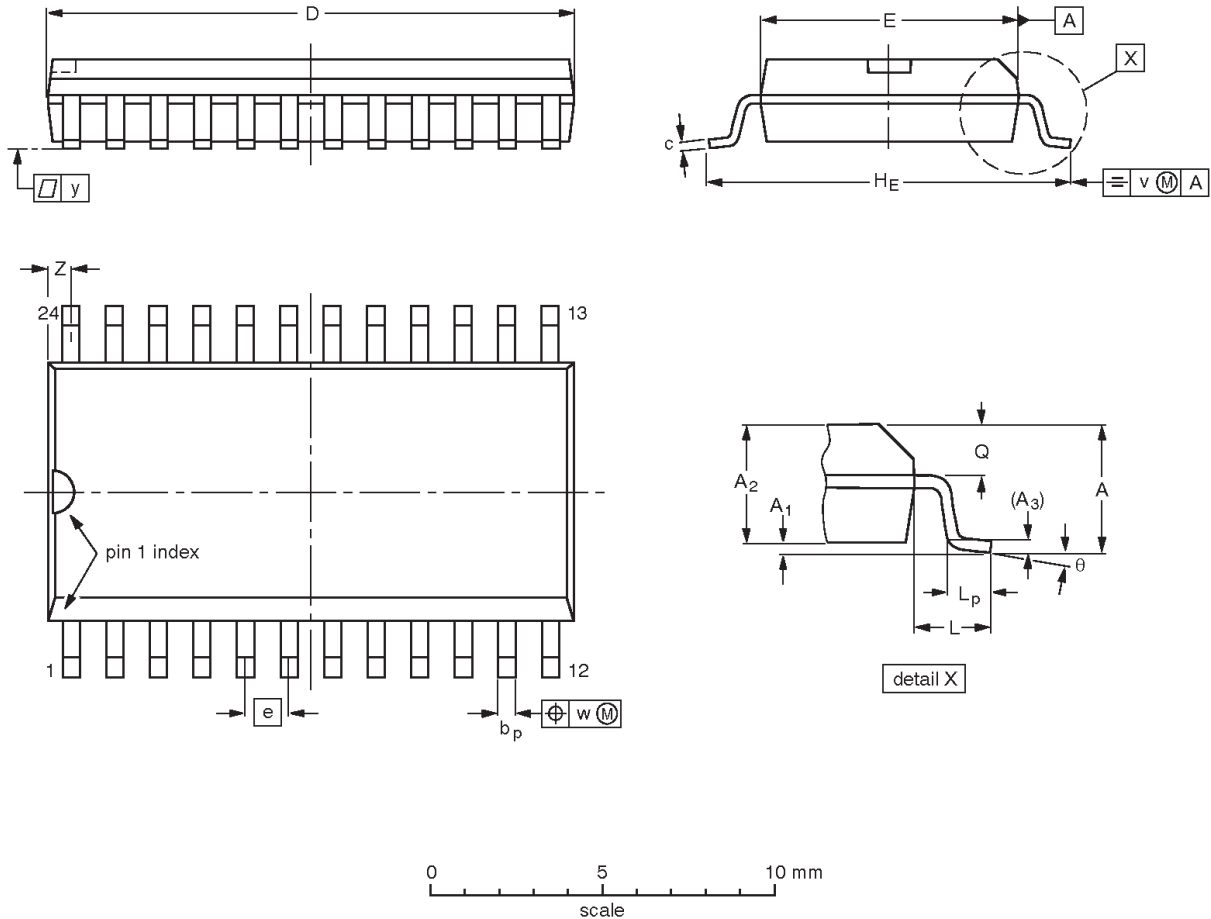
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001				99-04-28 99-12-27

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				-97-05-22 99-12-27

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

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